

Such  
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semiconductor structure comprising:

- an insulator layer;
- a conductive plug positioned within said insulator layer;
- a hard-stop layer located on said insulator layer;
- a non-conductive layer having an etched via and a conductive connector formed in said via in contact with said conductive plug;

The semiconductor structure of claim 1, wherein the first conductive layer is deposited in and on the second conductive layer including a portion in contact with the second conductive layer.

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semiconductor structure  
semiconductor structure  
and silicon carbide.

E1

conductor structure

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7. The semiconductor structure of claim 1, wherein said non-conductive layer comprises doped silicate glass.

E1

8. The semiconductor structure of claim 7, wherein said doped silicate glass comprises borophosphosilicate glass.

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B3

9. The semiconductor structure of claim 2, wherein said first conductive layer comprises one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

E1

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10. The semiconductor structure of claim 1, further comprising a substrate with a connection region, wherein said conductive plug is provided over said connection region.

11. A semiconductor device comprising:  
at least one memory cell comprising:

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B2

an active region in a substrate;  
a conductive plug positioned within an insulator layer and provided on said active region, said conductive plug being in contact with said active region;  
an etch-stop layer deposited on said insulator and around said conductive plug;  
an intermediate non-conductive layer provided over said etch stop layer and having an etched via over said plug; and  
at least one conductive layer in said via in electrical connection with said plug.

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12. The semiconductor memory device of claim 11, wherein said at least one conductive layer comprises:

a first conductive layer formed in said etched via, said first conductive layer including a portion in contact with said conductive plug; and

5 a second conductive layer deposited over and in contact with said first conductive layer.

13. The semiconductor memory device of claim 11, wherein said intermediate layer comprises doped silicate glass.

14. The semiconductor memory device of claim 13, wherein said doped silicate glass comprises borophosphosilicate glass.

15. The semiconductor memory device of claim 12, wherein said first conductive layer comprises one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

16. The semiconductor memory device of claim 12, wherein said second conductive layer comprises one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, titanium, titanium nitride and tungsten.

17. The semiconductor memory device of claim 11, further comprising an array of said memory cells.

18. A semiconductor device comprising:  
a conductive element;

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21. The semiconductor device of claim 20, wherein said doped silicate glass comprises borophosphosilicate glass.

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23. The semiconductor device of claim 18, further comprising a conductive layer located in said via.

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25. A processor-based system comprising:

a processing unit;

a semiconductor circuit coupled to said processing unit, said semiconductor circuit comprising:

a substrate supporting a connection region;

a conductive plug positioned within an insulator and provided on said connection region;

an etch-stop layer deposited on said insulator, said etch-stop layer being at the same level as a top portion of said conductive plug;

an intermediate non-conductive layer provided over said etch-stop layer and having an etched via over said conductive plug; and

a conductive connector electrically coupled to said connection region, said conductive connector comprising a first conductive layer deposited in and in contact with said etched via, said first conductive layer including a portion in contact with said conductive plug.

26. The processor-based system of claim 25, wherein said conducting connector further comprises a second conductive layer deposited over said first conductive layer, a semiconductor die being electrically connected to said conductive connector.

27. The processor-based system of claim 26, wherein said connection region comprises a doped region within said substrate.

28. The processor-based system of claim 26, wherein said intermediate layer comprises doped silicate glass.

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B4

Sub  
A5

Sub  
C4

29. The processor-based system of claim 28, wherein said doped silicate glass comprises borophosphosilicate glass.

30. The processor-based system of claim 26, wherein said first conductive layer comprises at least one layer of one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

31. The processor-based system of claim 26, wherein said second conductive layer comprises at least one layer of one or more materials selected from the group consisting of aluminum, copper, doped polysilicate, tantalum, tantalum nitride, titanium, titanium nitride and tungsten.

32. The processor-based system of claim 26, further comprising a substrate, and wherein said connection region is located in said substrate, and wherein said conductive plug is located over said connection region.

33. A method of making a semiconductor device, said method comprising:  
forming a layer of insulating material over a substrate;  
forming a conductive plug within said first layer of insulating material;  
forming an etch-stop layer over said first layer of insulating material and around said conductive plug;  
forming a second layer of insulating material over said conductive plug and etch-stop layer;  
etching said second layer of insulating material to said conductive plug and etch-stop layer to form a via.

34. The method of claim 33, further comprising depositing at least a first  
conductive layer in said via.

35. The method of claim 34, comprising depositing a second conductive layer over  
said first conductive layer in said via.

5 36. The method of claim 33, wherein said plug is formed by:  
forming an opening in said first layer of insulating material;  
depositing a conductive material on said first layer of insulating material, filling  
said opening; and  
10 abrading said conductive material from the top surface of said first layer of  
insulating such that only conductive material within said opening remains.

37. The method of claim 36, wherein said abrading comprises chemical-mechanical  
polishing of said conductive material.

38. The method of claim 36, wherein said conductive plug is connected to a doped  
region in said substrate.

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